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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,902	09/05/2003	Keiichiro Hirata	16869G-086400US	1545

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EXAMINER	
PATHAK, SUDHANSHU C	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,902	HIRATA ET AL.	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *September 5th, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *Sept. 5th, 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-to-4 are pending in the application.

Specification

2. The disclosure is objected to because of the following informalities:

The disclosure includes the title of the invention (application) on the same sheet along with the abstract; the title should be removed.

Appropriate correction is required.

Claim Objections

3. Claim 1 is objected to because of the following informalities:

Claim 1 on line 7, discloses "(clock)", it is not clear as to what this represents. The applicant is advised to delete "(clock)". Appropriate correction is required.

4. Claim 4 is objected to because of the following:

Claim 4, on line 1 discloses "The electronic device of claim 1...", however Claim 1 refers to "A synchronization control method...", therefore Claim 4 is a hybrid claim. The claims should either describe an apparatus for a particular function or a method for carrying out a process. Both method and apparatus cannot be specified in the same claim. The applicant is advised to amend the language of claim 4 so as to be consistent with the language of claim 1 or change the dependency of claim 4 so as to be consistent with claim 3.

For the purposes of claim rejections below, Claim 4 is interpreted to depend on claim 3 i.e. "The electronic of claim 3....".

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (2004/0025090) in view of Kucharewski et al. (7,073,001).

In regards to Claim 1, Miller discloses a synchronization control method for electronic device connectable to a serial interface, said synchronization control method (Abstract, lines 1-8) comprising: said electronic device monitoring synchronous state of a data reception timing clock generated by said electronic device itself with respect to said extracted clock component (Fig. 2A, element 100 & Fig. 2B & Fig. 4, element 400, 201 & Specification, Page 1, Paragraph 4, lines 1-12 & Specification, Page 1, Paragraph 7, lines 1-10 & Specification, Page 2, Paragraphs 19-20, 25-26) {Interpretation: The reference discloses a serial interface monitor so as to monitor the extracted clock component (Fig. 2B, element 209 & Fig. 4, element 201) and the internally generated clock of the electronic device (Fig. 2B, element 211 Fig. 4, element 201), wherein the synchronous state is monitored between the clocks i.e. absence of either clock, variation between clocks}. However, Miller

does not explicitly disclose extracting clock component from information flowing on the interface when the device is not receiving data.

Kucharewski discloses multiple transceivers transmitting and receiving data employing serial channels (Column 1, lines 47-49) {Interpretation: serial channel is interpreted as serial interface}. Kucharewski further discloses synchronizing the transmit / receive transceivers wherein the transmitter transmits a locking signal so as to establish a synchronized connection (Column 1, lines 40-55) {Interpretation: The reference discloses a synchronization process so as to provide alignment of the data (bit streams) at the receiver, by transmitting a locking signal which is interpreted as information}. Kucharewski further discloses performing synchronization between the transmitter and receiver before transmitting data (Column 1, lines 50-54) {Interpretation: The reference discloses performing synchronization before transmitting i.e. the receiver extracts the clock (synchronization) as is also referred in the instant specification on Page 1, Paragraph 4, when data is not received}. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Kucharewski teaches extracting clock signal when no data is received and this is implemented in the synchronization method as described in Miller so as to provide a robust (reliable) data transfer and prevent data loss as the receiver deviates in clock alignment while transferring data, and also confirms the received data is received.

In regards to Claim 2, Miller in view of Kucharewski discloses a synchronization control method for an electronic device connectable to as serial interface as described above. Miller further discloses the method further comprising: when said electronic device has detected that a clock made up of said clock component extracted from said information flowing on said serial interface is out of synchronization with said data reception timing clock generated by said electronic device itself, said electronic device performing self-synchronization operation such that said timing clock generated by said electronic device itself synchronizes with said clock made up of said extracted clock component (Abstract, lines 3-8 & Fig. 4, element 402 & Specification, Page 2, Paragraph 23, lines 20-25 & Paragraphs 24-25) {Interpretation: The reference discloses performing rate matching which is synchronization between the locally generated clock and the extracted clock, the details of which are disclosed in the paragraphs as mentioned above.}. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Miller in view of Kucharewski satisfies the limitations of the claims.

In regards to Claim 3, Miller discloses an electronic device (Fig. 2A, element 100 & Fig. 4) comprising a serial interface (Abstract, lines 1-2 & Specification, Page 1, Paragraph 3, 4 lines 1-3 & Fig. 2B, 4) {Interpretation: The reference discloses implementing the serial communication interface circuitry (Fig. 2B, 4) to be implemented in the loop network devices (Fig. 2A, 100)}; circuitry configured to generate a timing clock (Fig. 4, element 404);

and a synchronization control circuitry configured to extract a clock component from information present on said serial interface, and monitor a synchronous state of said timing clock generated by said electronic device itself with respect to said extracted clock component ((Fig. 2A, element 100 & Fig. 2B & Fig. 4, element 400, 201 & Specification, Page 1, Paragraph 4, lines 1-12 & Specification, Page 1, Paragraph 7, lines 1-10 & Specification, Page 2, Paragraphs 19-20, 25-26) {Interpretation: The reference discloses a serial interface monitor so as to monitor the extracted clock component (Fig. 2B, element 209 & Fig. 4, element 201) and the internally generated clock of the electronic device (Fig. 2B, element 211 Fig. 4, element 201), wherein the synchronous state is monitored between the clocks i.e. absence of either clock, variation between clocks}. However, Miller does not explicitly disclose extracting clock component from information flowing on the interface when the information is not addressed to the electronic device.

Kucharewski discloses multiple transceivers transmitting and receiving data employing serial channels (Column 1, lines 47-49) {Interpretation: serial channel is interpreted as serial interface}. Kucharewski further discloses synchronizing the transmit / receive transceivers wherein the transmitter transmits a locking signal so as to establish a synchronized connection (Column 1, lines 40-55) {Interpretation: The reference discloses a synchronization process so as to provide alignment of the data (bit streams) at the receiver, by transmitting a locking signal which is interpreted as information}. Kucharewski further discloses performing synchronization

between the transmitter and receiver before transmitting data (Column 1, lines 50-54) {Interpretation: The reference discloses performing synchronization before transmitting i.e. the receiver extracts the clock (synchronization) as is also referred in the instant specification on Page 1, Paragraph 4, when data is not received}. Kucharewski further discloses multiple devices (transceivers) in loop wherein only one of the devices can initiate synchronization and the remaining transceivers are subject transceivers (Fig. 2 & Column 4, lines 13-24) {Interpretation: The reference discloses a loop configuration similar to the Miller reference wherein one of the devices is a master (initiates sync process) and the other are slave devices}. Kucharewski further discloses the locking signal transmitted is transmitted / received by all the transceivers in the loop (Column 4, lines 27-60) {Interpretation: The initializing transceiver transmits the locking signal which propagates through all the devices in a loop thus synchronizing all the transceivers, therefore, the locking signal (information) is not addressed to any specific transceiver}. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Kucharewski teaches extracting clock component from information flowing on the interface when the information is not addressed to the electronic device and this is implemented in the device as described in Miller so as to provide a robust (reliable) data transfer and prevent data loss as the receiver deviates in clock alignment while transferring data, and further provide a generic signal (information) to synchronize all the transceivers in the loop.

In regards to Claim 4, Miller in view of Kucharewski discloses an electronic device as described above. Miller further discloses said synchronization control circuitry is further configured to synchronize said timing clock with said extracted clock component in response to determining that said timing clock is out of synchronization with said extracted clock component (Abstract, lines 3-8 & Fig. 4, element 402 & Specification, Page 2, Paragraphs 23-25) {Interpretation: The reference discloses performing rate matching which is synchronization between the locally generated clock and the extracted clock}. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Miller in view of Kucharewski satisfies the limitations of the claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, it is recommended to the applicant to amend all the claims so as to be patentable over the cited prior art of record. A detailed list of pertinent references is included with this Office Action (See Attached "Notice of References Cited" (PTO-892)).
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571)-272-3042.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sudhanshu C. Pathak
Examiner
Art Unit 2611